ELECTRONIC ENGINEERING
UCL

# A Wireless Digital Communications Link

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**Abstract**

The aims were to evaluate the suitability of two systems for a wireless digital communications system to link two buildings that are 275m apart. Originally, neither of the systems met the BER specified.

Some of the specifications were definite, whereas others were assumptions/suggestions that could be altered - in particular the noise figure (11dB) being greater than the receiver amplifier gain (10dB) resulting in a situation where noise is added at the receiver. Some of the specifications were altered so that system 2 satisfied the BER.

After the adjustments the BPSK was simulated as a vehicle for understanding the Xilinx block set. Furthermore, the 16-QAM system was simulated and the results show the expected constellation diagram. However, the trace shows the movement between each point on the constellation.

## Contents

# 1 Introduction

## 1.1 Aim

A wireless point – to – point digital communications link was to be developed, meeting the specifications in [1]. Two systems were given to be analysed, and the aim was to deem which, if any, was suitable to meet the requirements.

The chosen system was then to be simulated, using the Simulink software. The completed simulation could be used to program a Field Programmable Gate Array (FPGA), which would implement the solution. The device could be tested to see how far the physical implementation met the required specifications.

## 1.2 Specifications

The specifications at were to be met have been reproduced below from [1], with indications to which of them were fixed requirements, and which parameters could be changed according to the needs of the design.

Fixed Specifications

- Range : 275m
- Transmission Band: ISM (2.4GHz) band
- Bit Rate: 10Mbit/s
- Maximum Bandwidth: 5MHz
- Bit Error Rate: $< 10^{-4}$

Specifications that could be altered as needed

- Maximum Transmit Power: -2dBm
- Transmit Antenna: Isotropic
- Receiver Antenna Gain: 3dB
- Receiver Amplifier Gain: 10dB (operating at 20° ) with a noise figure of 11dB

## 1.3 Background Information

### 1.3.1 Data Rate and Bandwidth

A purely digital waveform has an infinite bandwidth. The transmission bandwidth for a digital communications system is limited by the transmission medium. Generally, the greater the bandwidth, the greater the cost of the system. Limiting the bandwidth creates distortions, so every system has a minimum bandwidth requirement to ensure the signal can be properly reconstructed at the receiving end.

The **symbol rate** is limited by the available transmission medium bandwidth. The theoretical maximum symbol rate is twice the medium bandwidth [otung].

### 1.3.2 Bit Rates and Symbol Rates

In a binary system, the symbol rate is the same as the bit rate, since each symbol is represented by one bit. The bit rate of a system however, can be increased by using multi-level digital modulation. Here a number of bits (n) are grouped together, and each group is represented by a single symbol. The data sequence is now represented by $2^n$ different symbols. The bit rate is now n × symbol rate.

## 2. The Given Systems

### 2.1 System 1

The given system has been reproduced below for analysis.

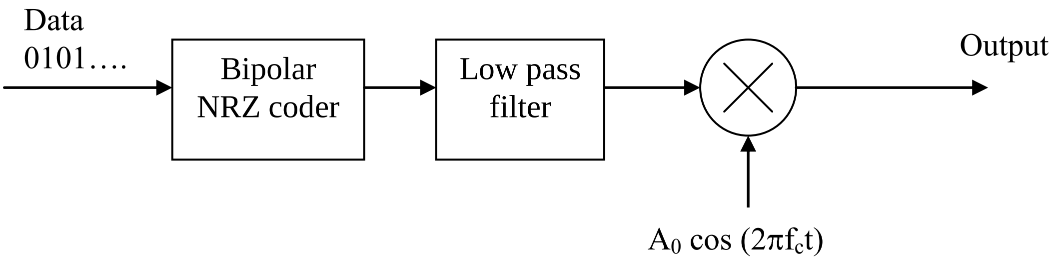

Figure 2.1 System 1 [1]

### 2.1 Analysis of System 1

The input binary data sequence is first fed into a Bipolar NRZ coder. The resulting sequence is a binary waveform in which a binary '1' is represented by a positive voltage (for example +1V) and a binary '0' is represented by an equal negative voltage (-1V). The low pass filter is used for pulse shaping. The resulting analogue wave is then modulated onto a carrier $A_0 \cos(2\pi f_C t)$.

When the modulating signal is at a +1V, the carrier wave passes through the modulator with the same amplitude and no phase shift. When the modulating signal is at -1V, the carrier wave at the output of the modulator has the same amplitude, but is shifted in phase by a 180°.

System 1 is therefore considered to be **Binary Phase Shift Keying (BPSK)**.

#### 2.1.1 Bandwidth Capabilities

The bandwidth of the modulated BPSK signal is twice the baseband bandwidth. Because the symbol rate is equal to the bit rate in this case, the theoretical maximum symbol rate that can be achieved with a 5MHz bandwidth is 10Mbit/s. In a practical implementation, once noise, interference and signal degradation effects start to appear, it would not be possible to receive a 10Mbit/s digital signal limited to only 5MHz.

#### 2.1.2 Bit Error Rate

The Bit Error Rate of a BPSK signal is given by:

$$BER = \frac{1}{2} erfc\left[\sqrt{\frac{E_b}{N_o}}\right] \text{ [otung]}$$

As can be seen from Figure 2.2, for the required bit error rate of $< 10^{-4}$, an $\frac{E_b}{N_0}$ ratio of approximately 8 is required.

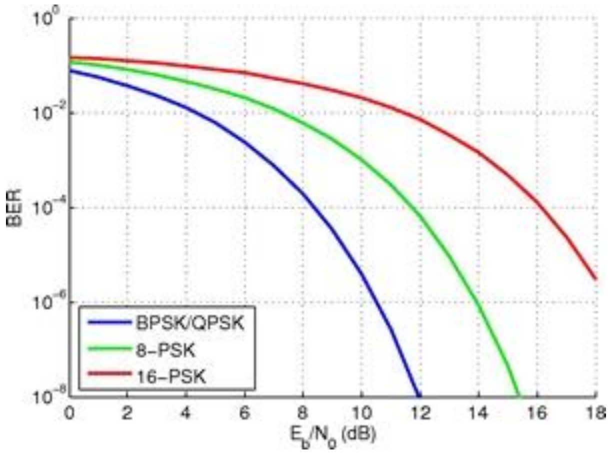

Figure 2.2 BER verses $E_b/N_0$ graph showing the relationships for 3 different PSK systems [site]

### 2.2 System 2

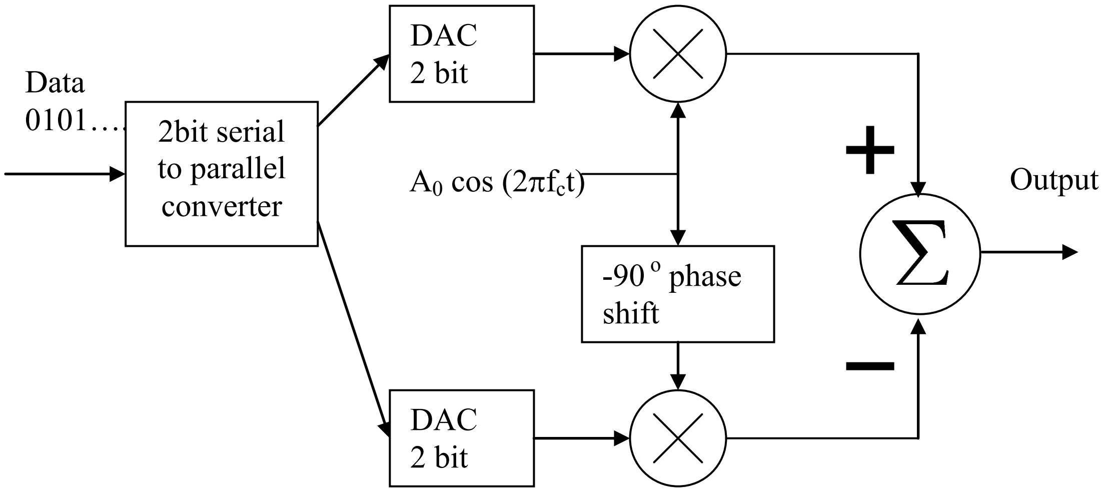

Figure 2.3 System 2 [1]

The system in figure 2.3 take in a serial bit of data, and converts it into two parallel data streams. The data from each stream in then taken in, 2 bits at a time, by a DAC. The DAC reads the two bits, and outputs a voltage level relative to the binary value of the input bits. 4 different levels are given out by each of the DACs. These waveforms are then used to modulate the carrier wave. The signal from one arm of the system is used to modulate a cosine version of the carrier (with 0 phase shift – "In phase" component). The signal from the other arm is used to modulate a sine version of the carrier (90° phase shift – "In quadrature component"). The modulated signals from the two arms are added together to give the QAM signal.

### 2.2.1 Bandwidth Capabilities

The maximum achievable symbol rate is limited by the bandwidth available. In this system, a lower symbol rate is required than the BPSK, because one symbol is now represented by 4 bits. The lower symbol rate will use up a smaller bandwidth, and so the system should be able to comfortably transmit 10Mbit/s in the given 5MHz bandwidth.

### 2.2.2 Bit Error Rate

The bit error rate for 16 QAM is given by

$$BER = \frac{2}{\log_2 M}\left[1 - \frac{1}{\sqrt{M}}\right] erfc\left[\sqrt{\frac{3E_b \log_2 M}{2(M-1)N_0}}\right] \text{ [otung]}$$

Where M is the number of levels, 16 in this case. From a similar graph as Figure 2.2, given in [otung], the required $\frac{E_b}{N_0}$ (dB) ratio = 13.

## 3 Improved Specifications

Since the BER of both of the system does not meet the requirement of $10^{-4}$ and BPSK doesn't meet the bit rate requirement, we decide to alter some of the specification and focus on 16QAM. To do this efficiently, we know that BER is directly dependant on the $\frac{E_b}{N_o}$, so started from the desire value of $\frac{E_b}{N_o}$ and worked backward.

We assume that the noise of the whole system is the thermo noise from the transmitter and receiver and the noise figure of the amplifier.

The signal to noise ratio is related to $\frac{E_b}{N_o}$ by the relationship below:

$$\frac{E_b}{N_o}K = \frac{S}{N}$$

$$\frac{E_b}{N_o} = \frac{\frac{S \times A}{T_b}}{\frac{N}{B}} = \frac{S \times A}{T_b} . \frac{B}{N} = \frac{S}{N} . \left(\frac{AB}{T_b}\right)$$

As $S/N$ is the SNR and assuming $K = \frac{T_b}{AB}$

Then $\frac{E_b}{N_o} = \frac{SNR_{out}}{K}$

$T_b = 10^7$ bit/s

$B = 5 \times 10^6$ Hz

For 16QAM

$$A = \frac{P_{average}}{P_{peak}} = \frac{314.4\mu w}{631\mu w} \cong 0.5$$

$$K = \frac{T_b}{A.B} = \frac{10^7}{5 \times 10^6 \times 0.5} = 4$$

For 16 QAM; in order to achieve a BER< $10^{-4}$ ; then $\frac{E_b}{N_o}$ is roughly equal to 13, obtained graphically.

$$\text{Hence } \frac{E_b}{N_o} = \frac{SNR_{out}}{K} \Rightarrow 13 = \frac{SNR_{out}}{4} \Rightarrow SNR_{out} = 52dBm$$

$$NF = SNR_{in} - SNR_{out}$$

Assuming NF=3.3 dB ( a typical value and components exist with this value)

$$SNR_{in} = NF + SNR_{out} = 3.3 + 52 = 55.3dBm$$

$$SNR_{in} = Singal - Noise = P_{Rx} - N$$

$$N = 4kTB = -100.9dBm$$

$$\Rightarrow P_{Ex} = SNR_{in} + N = 55.3 - 100.9 = -45.6dBm$$

However the received power is has been through some reductions and gains

$$P_{Rx} = P_{Tx} + P_{pathloss} + P_{reciever\ gain}$$

As was calculated before by arwa ; the pathloss was -88dBm. We found a receiver that can provide a receiver gain of 32 and amplifier with 10dB gain and NF=3.3

Hence

$$P_{Rx} = P_{Tx} + P_{pathloss} + P_{reciever\ gain}$$

$$\Rightarrow -65.6 = P_{Tx} - 88 - 32$$

$$\Rightarrow P_{Tx} = 10.4dBm$$

The maximum allowed transmitter power is 20dBm (100mW) hence we are in the legal range.

Hence the Improved Specification

- Bit rate = 10Mbit/s
- Maximum bandwidth 5 MHz
- Bit Error Rate <$10^{-4}$
- Maximum Transmit Power = 10.4dBm
- Transmit antenna - isotropic
- Receiver antenna Gain = 32dB
- Receiver amplifier gain = 10dB (operating at room temp 20$^{O}$C), with a noise figure of 3.3dB.

# 4 Simulations

There are numerous simulation packages available for wireless system evaluation. These include the Omnet++, Simulink as well as other open source projects. However, due to time constraints it was believed that using an organized package should be used. Moreover, due to the FPGA implementation requirement, a simulation package was to be used which could be easily transferred to the FPGA. Xilinx package is a simulink toolbox extension developed by Xilinx Inc. The simulation blocks that are available in Xilinx can be completely transferred to a programmable FPGA. The Nalltech Xtreme DSP was readily available in the Laboratories. As the 16-QAM simulation was believed to be harder to regenerate, a BPSK simulation was implemented initially using Xilinx. In the following sections the BPSK simulation will be examined and it will be followed by the 16-QAM implementation.

## 4.1 BPSK Simulation

The Block Diagram

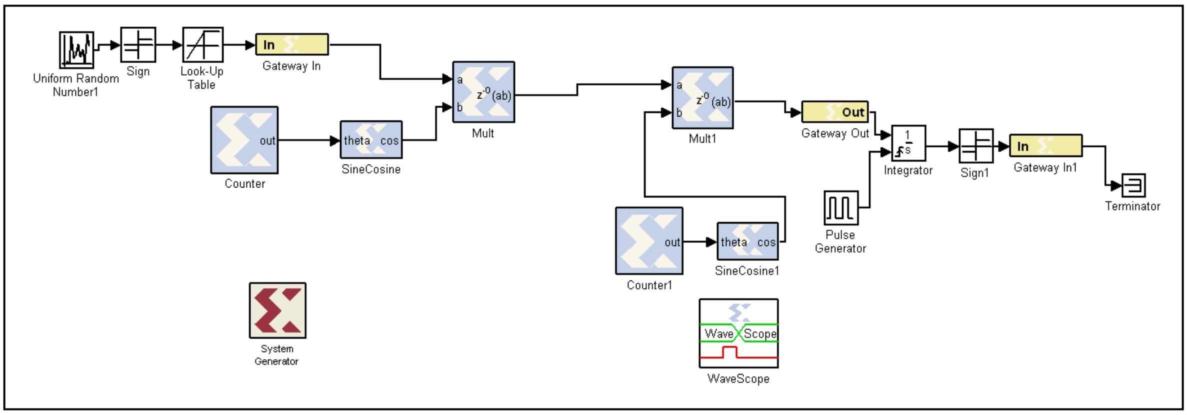

Figure 4.1. The implementation of BPSK in Simulink using the Xilinx Blockset.

### 4.1.1 The Transmitter

In a BPSK system; the binary input data of 0 and 1 is multiplied by the carrier frequency to generate a phase shift. Hence a data input of '1' corresponds to a cosine wave and '0' corresponds to cosine wave with $180^0$ phase shift. A cosine phase shifted by $180^0$ is identical to multiplying the cosine by '-1'.

$$-\cos(wt)=\cos(wt+\pi)$$

The first block generates random binary numbers in the range [-1,1]. The second block puts them in discrete values of [-1,0,1]. The third block , look-up table , has the input [-1,0,1] and outputs [-1,1,1]. That is , it switches all the zeros to one.

These three blocks are simulink blocksets and cannot be implemented on an FPGA. Hence, if implemented it should be fed in from gate in of the FPGA. Therefore the Gate In block enables us to embed simulink blocks on a Xilinx implementation. Though this usage is not preferred, nevertheless it enables a software simulation. Hence at the Gate In output, a pseudo random generation of [-1,1] is created.

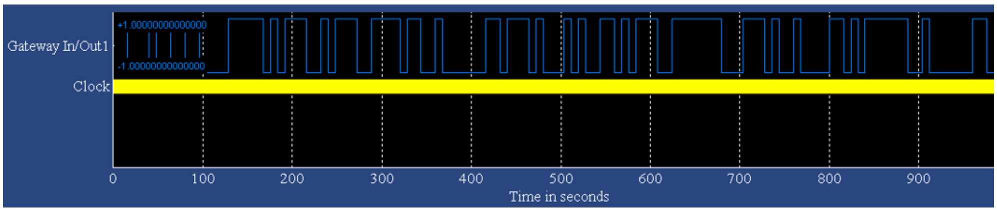

Figure 4.2 Random generation of [-1,1].

The System generator is a compulsory block and it is required for every Xilinx simulation. The System Generator block provides control of system and simulation parameters, and is used to invoke the code generator. Once a System Generator block is added to a model, it is possible to specify how code generation and simulation should be handled.

The wavescope is used to view the block inputs and outputs. If a signal is shown on wavescope, it should appear identically on the FPGA.

To generate the cosine waves in Xilinx two blocks are required. The counter block counts in steps up to a specific number and drops back to zero. Hence a 5-bit counter will count up to 31 and drop back to zero.

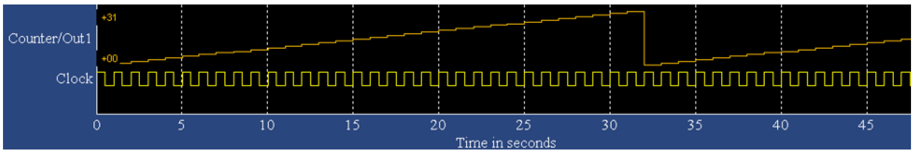

Figure 4.3 The output of the counter blocks

The sine/cosine block is can implement a cosine function up to a certain frequency. Hence the frequency of the cosine wave will be dependant on the counting steps. The figure below shows this relationship.

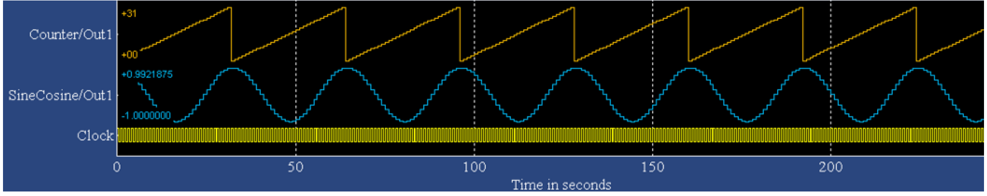

Figure 4.4 Comparison of the counter block to the output of the cosine generator.

At this point there is a random [-1,1] generation as well as a cosine wave. Hence using a multiplier a BPSK system can be achieved.

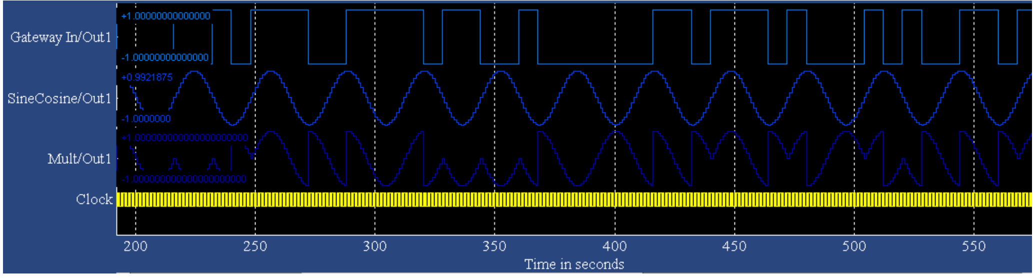

Figure 4.5 A BPSK signal.

### 4.1.2 The Receiver

In order to retrieve a BPSK signal it has to be multiplied by the carrier frequency and then integrated over the period time.

The period of integration is specified by the pulse block. The sign block outputs [-1,0,1] for negative, zero and positive numbers. Hence to see the performance of the BPSK the input and output data is shown below:

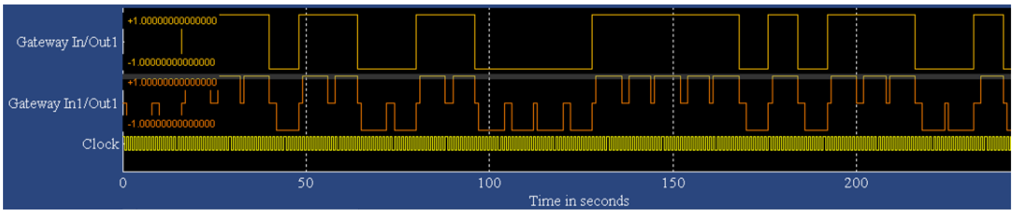

Figure 4.6 Comparison of the input to output signal.

## 4.2 16-QAM Simulation

The simulation of BPSK provided a perfect start for familiarization of Xilinx. Simulation of 16-QAM is done in three parts. The Xilinx blockset was used to generate the baseband signal. However, the

FPGA could not generate a carrier of 2.4GHz. Hence an Agilent E4432B carrier generator was used to generate the carrier and Rohde & Schwarz signal analyzer to generate a constellation diagram. In the next section each block and its parameter of the Xilinx implementation is explained followed by a description of the Agilent Signal Generator and finally results of the 16-QAM from the signal analyzer is plotted.

### 4.2.1 The Block Diagram

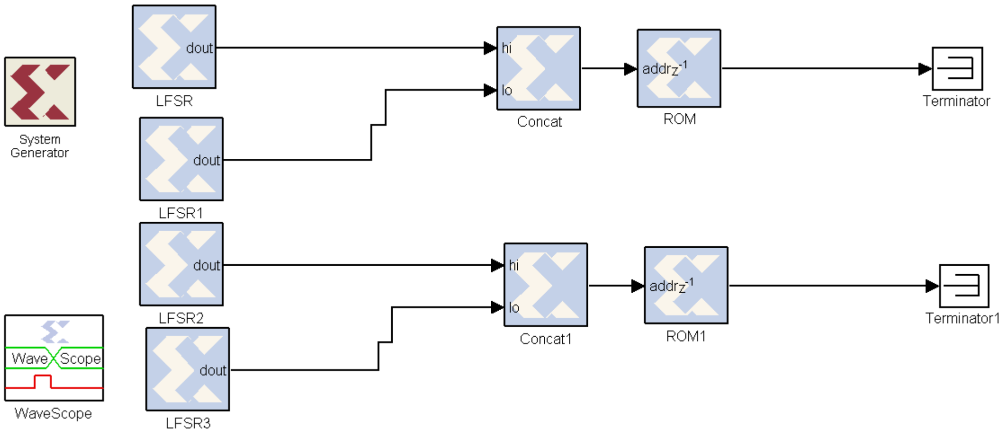

Figure 4.7. The block diagram of Xilinx Implementation of 16-QAM.

#### 4.2.1.1 LFSR

Although the specifications required one stream of data to be input to the system, it was not possible to implement the serial to parallel block using Xilinx due to time constraints. Instead two streams of data was generated (as if it coming out of the Serial-parallel output).
Generation of random zeroes and one was done using the Linear Feedback Shift
Register (LFSR). The operation of an LFSR can be found in other documents but the important parameters are the number of bits, the tap location and the seed. Table 1 shows the various values used:

| LSFR Number | Number of bits | Tap Location | Seed |
|---|---|---|---|
| LFSR | 15 | F1 | 3F |
| LFSR1 | 15 | F1 | 1F |
| LFSR2 | 15 | F1 | 2F |
| LFSR3 | 15 | F1 | 4F |

Table 4.1. The parameters in the LFSR blocks in the Xilinx implementation of 16-QAM

The graph below shows the random generation of [0,1] sequence using the LFSR block in Xilinx:

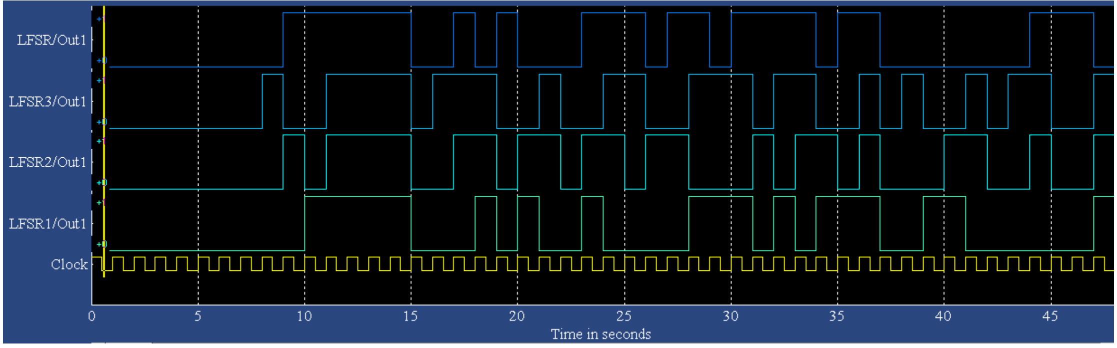

Figure 4.8. The output of different LFSRs for random [0,1] generation.

#### 4.2.1.2 Concat

The concat block takes two bits first from the high input and second from the low input and combines them together. As a result a 2 bit word is generated. This operation is carried out on both streams of data. The figure below shows the inputs of the concat block and its output for the first stream of data.

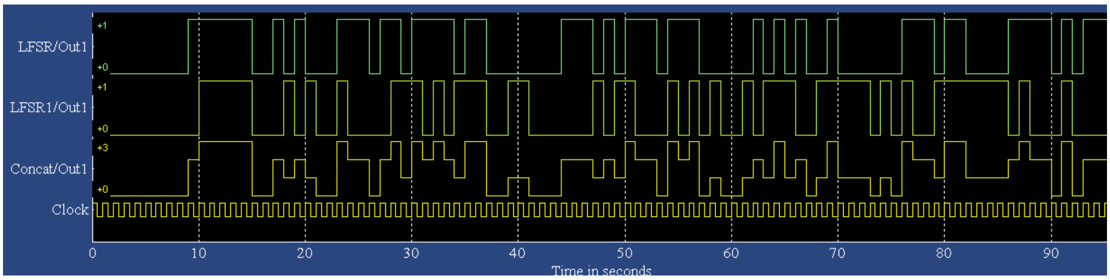

Figure 4.9. The inputs and outputs of concat block.

### 4.2.1.2 ROM

The ROM block is a single port read-only memory. So far , its been possible to generate a 2bit word. However, it is required to assign these words to specific symbols. The ROM block will take these input values and assign them to specific symbols.

| 2 bit word | Symbol |
|---|---|
| 00 | -1 |
| 01 | -0.3 |
| 10 | 0.3 |
| 11 | 1 |

Table 4.2. The ROM assignment table.

In Table 2, the assignment table is listed. The symbol values are arbitrary and could be any value. It is necessary to have equal spacing between the values to provide equal change of amplitude and phase.

The figure below shows the input and output of the upper stream data. It can be noticed that there is a delay in the signal. The delay is due to storage of data and then processing it. It can also be seen that the amplitude of the signal has changed from [0,3] to [-1,1].

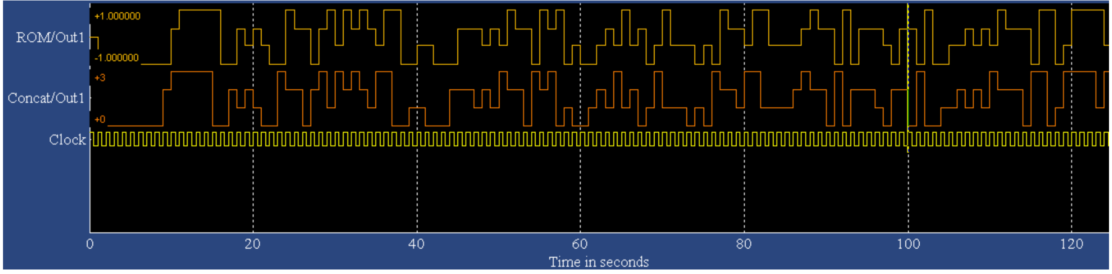

Figure 4.10 .The input/output of the upper ROM.

## 4.3 Final Remarks

The Xilinx blockset only creates the baseband signal. In order to transfer the blockset to the FPGA board, the system generator is used to implement circuit into one block. Transferring this block to the FPGA board can be carried out through a USB port.

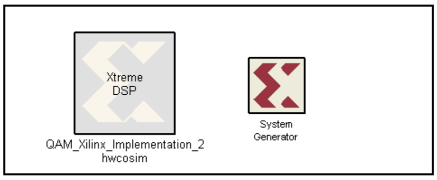

Figure 4.11. The block transferred to FPGA.

In order to multiply the baseband by the carried the data was transferred from the FPGA board to the Agilent E4432B carrier generator. The first stream of data was multiplied by a cosine carrier at 2.4GHz and the second stream was multiplied by the sine carrier at 2.4 GHz using the I and Q ports.

In order to investigate the output of the system, the Rohde & Schwarz signal analyzer was used. It produced the constellation diagram for the 16-QAM signal. The figure below shows the two carriers modulated with the data and its output on the constellation diagram.

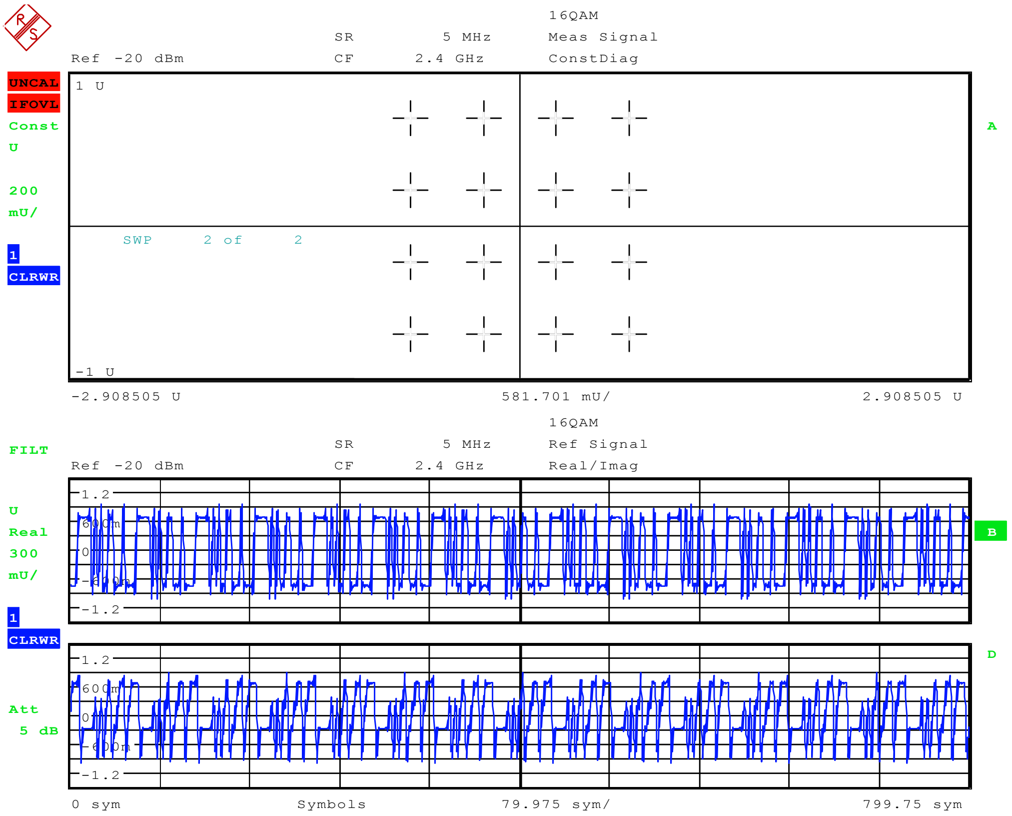

Figure 4.12. The constellation diagram (above) and the modulated ( below)

## 5 Conclusions

The 16Qam system that was simulated and evaluated was shown to meet the specified requirements. However, it is not necessarily an optimum solution and is by no means exclusive.

### References

[1] Mitchell JA . *Problem Brief 3.* University College London. 2007.
[2] Otung I. *Communication Engineering Principles* . Palgrave: New York. 2001.
[3] Various Publishers.: Wireless Facts and Fiction. Available at http://marconig.files.wordpress.com/2007/06/ber11.jpg